



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,310	02/26/2002	Motoki Kanamori	XA-9632	2808

7590 05/28/2003  
Miles & Stockbridge P.C.  
Suite 500  
1751 Pinnacle Drive  
McLean, VA 22102-3833

EXAMINER

PHAM, LY D

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/082,310

Applicant(s)

KANAMORI ET AL.

Examiner

Ly D Pham

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 1-3 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 4-7 and 10 is/are rejected.
- 7) ☒ Claim(s) 8 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This office acknowledges receipt of the following items from the applicant:  
  
Information Disclosure Statement (IDS) was considered.  
  
Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

#### *Election/Restrictions*

2. Claims 1 – 3 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.  
  
Election was made **without** traverse in Paper No. 5.
3. Claims 4 – 10 are presented for the examination.

#### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:  
  
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claims 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaki et al. (US Pat 6,549,974 B2).

Regarding **claim 4**, Kaki et al. disclose a non-volatile storage device comprising a controller (fig. 1, processor 2), a buffer memory (fig. 1, write buffer memory 5), and a non-volatile memory (fig. 1, flash memories 4),

Art Unit: 2818

wherein said buffer memory comprises plurality of banks (col. 4, lines 39 – 42, the storage capacity of the write buffer memory corresponds to a plurality of sectors in units of 512 bytes, which are considered as the plurality of banks); and

wherein in response to control information from an external unit (fig. 1, external data enter through standard bus 1 to processor 2), said controller stores first data into the banks of said buffer memory (abstract: data responsive to first write command) and then further stores the stored data into a specified area of said non-volatile memory (col. 5, lines 5 – 9 and 35 – 36. different chips of the flash memories further indicate specific non-volatile storage areas).

Inherently, the operation for the second write command (abstract) inherently includes the step of storing the second data to the buffer memory because it is required that before data are stored in flash memory, they have to be loaded into the write buffer memory (col. 4, lines 42 – 46).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made to note that, concurrently with the storage of data into said non-volatile memory, the controller stores second data, which is entered from the external unit, into said buffer memory from which data has been transferred to said non-volatile memory (abstract: data responsive to second write command get carried out in parallel with the data being in operation of the first write command. See also col. 9, lines 24 – 34).

Regarding **claim 5**, Kaki et al. further disclose a non-volatile storage device according to claim 4, wherein a total storage size of all banks of said buffer memory equals a size of a unit of data that is written into said non-volatile memory at a time (col. 5, lines 13 – 26).

Art Unit: 2818

Regarding **claims 6 and 7**, Kaki et al. also disclose a non-volatile storage device according to claim 4, further comprising:

a status register or a status flag indicating a completion/incompletion of the data transfer from said buffer memory to said non-volatile memory, wherein the status register or the status flag is controlled by said controller (col. 3, lines 37 – 58, status polling is utilized to determine that the operation of writing the data into the flash memory chip has ended/to determine completion of the erase operation .... See also col. 9, line 52 – col. 10, line 4).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaki et al. (US Pat 6,549,974 B2) in view of Tobita et al. (US Pat Pub 2002/0051394 A1).

Regarding **claim 10**, Kaki et al. further disclose a non-volatile storage device according to claim 4, further comprising:

a register in which an address range of said non-volatile memory is set (fig. 1, address controller 31, col. 4, lines 53 – 56).

Although Kaki et al. did not clearly disclose data storage error detection means for detecting whether or not data may be stored in said non-volatile memory based on the address information that is set in said register ...; however, this feature has been shown by Tobita et al. (paragraph 0329, "... data amount does not exceed a predetermined value" and paragraph 0036). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to integrate the feature of storage error detection according to data amount shown by Tobita et al. to the invention of Kaki et al. so that the non-volatile storage device would operate more efficiently.

Art Unit: 2818

*Allowable Subject Matter*

7. Claims 8 and 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

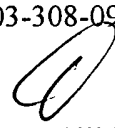
9. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham

May 18, 2003

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800